PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Assistant Commissioner for Patents
United States Patent and Trademark Office
Box PCT
Washington, D.C.20231
ETATS-UNIS D'AMERIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 22 May 2000 (22.05.00)	
International application No. PCT/SG98/00076	**Applicant's or agent's file reference** ST/61512
International filing date (day/month/year) 25 September 1998 (25.09.98)	**Priority date** (day/month/year)
Applicant DESPREZ-LE GOARANT, Yann et al	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

13 April 2000 (13.04.00)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland**	Authorized officer Pascal Piriou
Facsimile No.: (41-22) 740.14.35	Telephone No.: (41-22) 338.83.38

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
ST/61512		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/SG98/00076	25/09/1998	25/09/1998
International Patent Classification (IPC) or national classification and IPC H04N9/64		
Applicant STMICROELECTRONICS ASIA PACIFIC PTE LTD et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   ☐ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
13/04/2000	17.11.2000
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Montanari, M Telephone No. +49 89 2399 2602

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/SG98/00076

I. Basis of the report

1. This report has been drawn on the basis of *(substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments (Rules 70.16 and 70.17).)*:
Description, pages:

1-12 as originally filed

Claims, No.:

1-7 as originally filed

Drawings, sheets:

1/5-5/5 as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
- ☐ the language of publication of the international application (under Rule 48.3(b)).
- ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.
- ☐ filed together with the international application in computer readable form.
- ☐ furnished subsequently to this Authority in written form.
- ☐ furnished subsequently to this Authority in computer readable form.
- ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:

☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

(Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-7
	No:	Claims	
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-7
Industrial applicability (IA)	Yes:	Claims	1-7
	No:	Claims	

2. Citations and explanations
see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

The examination is being carried out on the **following application documents**:

Text for the Contracting States:
AT BE CH DE DK ES FI FR GB GR IT IE LI LU MC NL PT SE

Description, pages:

1-12 as originally filed

Claims, No.:

1-7 as originally filed

Drawings, sheets:

1/5-5/5 as originally filed

1. Reference is made to the following documents:

   D1: US-A-5339011
   D2: US-A-4689665

2. **Claim 1**

2.1 Document D1 discloses an RGB control circuit for use in television/video display control, comprising (see figure 1 and the relative description at column 5):

a display driver current sensor (R1);

a counter circuit (18) and analog output circuit (19, 12) coupled to control the display driver current;

a comparator (17) coupled with the display driver current sensor as input, for determining and outputting a measure of the difference between the sensed display driver current and a predetermined value thereof; and

a speeding logic circuit (see figure 11 and the relative description at column 11, lines 29 - column 12, line 42) coupled to the counter circuit, and arranged to

control the up/down counting rate of the counter circuit.

2.2 The circuit claimed in claim 1 differs from the above mentioned circuit only in that the counting rate of the counter circuits is increased according to the difference of display driver current measured by the comparator, which has a plurality of comparator circuits.

The problem to be solved by the present invention may therefore be regarded as how to adapt the circuit disclosed by D1 so that the speeding logic is active at all times and not only during the CRT warm up phase as disclosed by D1.

However, document D2 discloses a similar circuit, wherein the counting rate of the counters is controlled by means of a clock signal generator whose frequency is varied in dependence on the value of the comparator circuit output signal (see the passage from column 1, line 46 to column 2, line 10).

Therefore it appears to be a normal design possibility for the skilled person to include said feature in the circuit described in document D1 and thus to arrive at an apparatus according to claim 1.

Consequently, the subject-matter of claim 1 lacks inventive step (Article 33(3) PCT).

3. **Dependent claims**

3.1 The circuit indicated in the preceding paragraph resulting from the combination of the subject-matters of D1 and D2 would control the counting rate of the counters based on the output of the comparator so as to converge the display driver current to said predetermined value, i.e. to the voltage determined by R2 and R3 in figure 1 of D1.
Thus the subject-matter of **claim 2** lacks inventive step (Article 33(3) PCT).

3.2 As to **claim 3**, D1 discloses that during the warm up time the RGB outputs are blanked (see column 11, lines 16 to 28). Thus **claim 3** fails with claim 2 on which it depends.

3.3 The additional features disclosed in the **remaining dependent claims** appear to be minor circuit details which lie within the capabilities of the skilled person, and therefore they do not appear, at least for the time being, to add anything inventive to the subject-matter of the claims on which they depend.
Thus these claims fail with the claim on which they depend (Article 33(3) PCT).

4. The claims are not drafted in the proper two-part form (Rule 6.3(b) PCT).

5. Reference signs in parentheses are not inserted in the claims to increase their intelligibility, Rule 6.2(b) PCT.

6. Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the documents D1 and D2 is not mentioned in the description, nor are these documents identified therein.

7. A document reflecting the prior art described on pages 3 to 5 with reference to figures 1 to 3 is not identified in the description (Rule 5.1(a)(ii) PCT).

8. All claims fulfil the requirements of Article 33(4) PCT since the device concerned is widely applied in the television industry.

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H04N 9/64, 9/72

A1

(11) International Publication Number: WO 00/19727

(43) International Publication Date: 6 April 2000 (06.04.00)

(21) International Application Number: PCT/SG98/00076

(22) International Filing Date: 25 September 1998 (25.09.98)

(71) Applicants *(for all designated States except US)*: STMICROELECTRONICS ASIA PACIFIC PTE LTD [SG/SG]; 28 Ang Mo Kio Industrial Park 2, Singapore 569508 (SG). STMICROELECTRONICS S.A. [FR/FR]; 7, avenue Gallieni, F–94253 Gentilly Cedex (FR).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: DESPREZ–LE GOARANT, Yann [FR/SG]; 28 Ang Mo Kio Industrial Park 2, Singapore 569508 (SG). JAFFARD, Jean–Luc [FR/SG]; 4 bis, rue du Cotaire, F–38120 Saint Egrève (FR). MICHON, Christian [FR/FR]; 28 Ang Mo Kio Industrial Park 2, Singapore 569508 (SG).

(74) Agent: DONALDSON & BURKINSHAW; P.O. Box 3667, Singapore 905667 (SG).

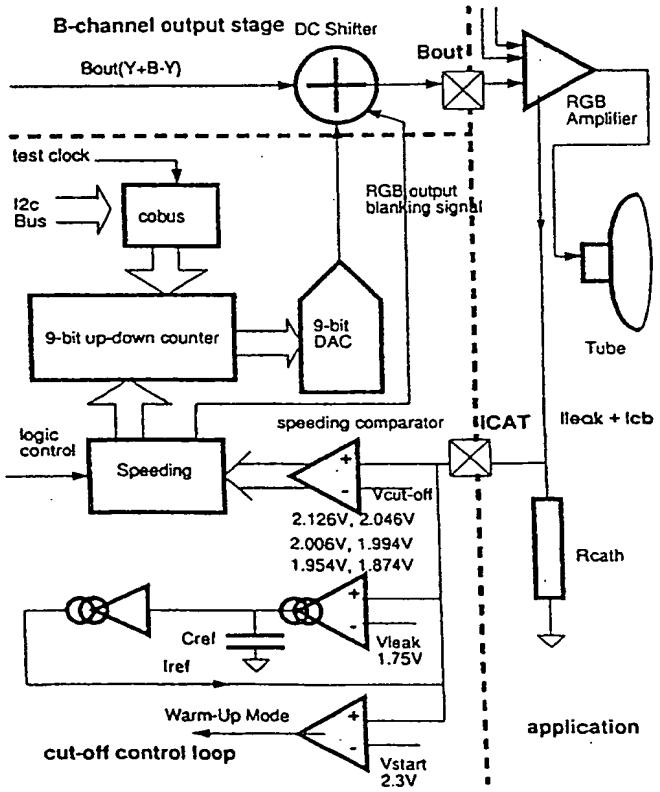
(81) Designated States: JP, SG, US, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: A DIGITAL CUT–OFF CONTROL LOOP FOR TV USING SPEEDING AND BLANKING CIRCUITS

(57) **Abstract**

An improved digital cut–off control loop for black level adjustment in a video processor for controlling RGB output signals. The improved circuit advantageously provides a higher resolution of the black level adjustment, and a short cut–off convergence time when the TV set is switched on. The improved circuit can also blank the RGB output when the cut–off control loop has not converged to the correct level.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

A DIGITAL CUT-OFF CONTROL LOOP FOR TV USING SPEEDING & BLANKING CIRCUITS

Field of the Invention

This invention relates to a television/video display control circuit, and in particular to a cut-off control circuit for use in a television RGB controller.

Background of the Invention

A cut-off control loop circuit in a television permits the automatic control of the cut-off point of the three RGB cathodes. The black level of the RGB signals is automatically adjusted to have the same cut-off current on each of the RGB cathodes, in order to have the proper DC level at each RGB cathode, for a correct colorimetry of low light level signals. The RGB cathode currents are sequentially measured at the output of the external video amplifier during the three cut-off lines. A conventional 8-bit digital cut-off control loop has low resolution of the black level adjustment, requires a relatively long time to reach cut-off stability when the TV set is switched on, and cannot blank the RGB output when the cut-off control loop is not stable. To increase the resolution to 9-bits leads to even longer convergence times of the cut-off loops.

Summary of the Invention

The present invention aims to address some of the difficulties associated with the prior art, and embodiments of the invention are able to provide an increased resolution of black level adjustment whilst having a short cut-off convergence time during initialisation and enabling blanking of the RGB outputs when the cut-off control loop does not converge to the correct level.

In accordance with the present invention, there is provided an RGB control circuit for use in

television/video display control, comprising: a display driver current sensor; a counter circuit and analog output circuit coupled to control the display driver current; a speeding comparator having a plurality of comparator circuits coupled in parallel with the display driver current sensor as input, for determining and outputting a measure of the difference between the sensed display driver current and a predetermined value thereof; and a speeding logic circuit coupled to the speeding comparator and counter circuit, and arranged to control the up/down counting rate of the counter circuit according to said measure of difference in display driver current.

The speeding logic circuit may be arranged to control the counting rate of the counter circuit, and thus the display driver current, based on the output of the speeding comparator so as to efficiently converge the display driver current to the predetermined value.

Preferably the speeding logic circuit produces a RGB output blanking signal whilst said display driver current is substantially different from said predetermined value. Preferably control circuits are provided for each of the colour (RGB) channels, wherein the speeding logic circuit produces the RGB output blanking signal based on the counting rate of any and/or each of the counter circuits for the colour channels.

Preferably the speeding comparator has a plurality of outputs including a convergent output and at least one upper output and lower output, wherein the convergent output corresponds to the display driver current being substantially equal to the predetermined value and the upper and lower outputs are utilised by the speeding logic circuit to determine the up/down counting rate of the counter circuit. In an preferred embodiment, each of the upper and lower outputs correspond to respective up and down binary counting rates for the counter circuit.

Brief Description of the Drawings

The invention is described in greater detail hereinafter, by way of example only, with reference to the accompanying drawings, wherein:

Figure 1 is a block diagram of a conventional 8-bit digital cut-off control loop for one channel of an RGB output controller;

Figures 2 and 3 are waveform diagrams;

Figure 4 is a block diagram of a digital cut-off control loop for one channel of an RGB output controller, in accordance with a preferred embodiment of the present invention; and

Figure 5 is a schematic block diagram of an implementation of speeding logic and up/down counter circuitry according to an embodiment of the invention.

Detailed Description

A conventional 8-bit digital cut-off control loop circuit is shown in block diagram form in Figure 1. In the drawing, only the BLUE channel circuitry is shown, the for which the red and green channels are the same. The cut-off control loop permits the automatic control of the cut-off point of the three RGB cathodes. The black level of the RGB signals is automatically adjusted to have the same cut-off current on each of the RGB cathodes. The RGB cathode currents are sequentially measured at the output of the external video amplifier during the three cut-off lines.

During the frame blanking pulse, the RGB outputs are blanked and the total cathodes leakage current *Ileak* is measured. The cathode current is input to the circuit at *ICAT*. An external measurements resistor *Rcath* is connected between the pin *ICAT* and the ground. During the leakage current measurement the circuit provides a controlled current *Iref* so that the total current (*Iref* + *Ileak*) through the external resistor *Rcath* reaches the reference leakage voltage *Vleak*, where:

$$Vleak = (Iref + Ileak) * Rcath$$

The maximum controlled current Iref that the circuit can provide is 200uA, and it is memorized by use of an internal capacitor *Cref*. The leakage reference voltage *Vleak* is 1.75V.

The cut-off current measurement is sequentially achieved for the channels during the three lines after the frame blanking (cut-off lines), as is illustrated in Figure 2. During the first cut-off line, a reference voltage is inserted on the blue channel output, the green and the red outputs are blanked. The total cathode current is the leakage current (previously measured) plus the blue cut-off current *Icb* is then present. If the voltage on the *ICAT* pin is not equal to the cut-off reference voltage (*Vcut-off*), the simple comparator will give an up or down signal to the 8-bit up-down counter so that the output current of the 8-bit DAC will automatically change until the voltage on the *ICAT* pin is equal to *Vcut-off*. Thus the circuit can adjust automatically the black level so that the voltage on the *ICAT* pin is equal to cut-off reference voltage (*Vcut-off*), wherein:

$$Vcut\text{-}off = (Iref + Ileak + Icb) * Rcath$$

The black level is memorized using the 8-bit up-down counter and the 8-bit DAC. The blue cut-off current is determined by the resistor *Rcath*, such that:

$$Icb = (Vcut\text{-}off - Vleak) / Rcath$$

The second cut-off line is used for the green channel cut-off adjustment (red and blue outputs are blanked) and the same manner as described above, and the last cut-off line is dedicated to the red channel cut-off adjustment (with blue and green outputs blanked). The cut-off control loop can adjust the black level in a range of 2V.

The beam current during the scanning can be relatively high, and in order to avoid high voltage on the *ICAT* pin, a clamping circuit will clamp the *ICAT* voltage to 2.5V. At the time of start-up, the circuit is in a warm-up detection mode, with waveforms similar to that illustrated in Figure 3. When the TV set is switched on, the cut-off control loop is not active, and during the three cut-off lines a white level is inserted on the RGB outputs in order to avoid a white flash on the screen at the start. As soon as the start beam current *Istart* is detected on the *ICAT* pin, the cut-off control loop becomes active and the cut-off levels are

inserted during the three cut-off lines, where:

$$Istart = (Vstart - Vleak) / Rcath \qquad Vstart = 2.3V$$

The sensing of the start beam current is achieved during a small window at the middle of the cut-off lines.

Conventional cut-off control loop circuits of the type described above and illustrated in Figure 1 have a number of drawbacks, some of which are summarised below:

1) Low resolution of the black level adjustment.
Generally, the range of the black level adjustment is about 2V. Since there is total 256 steps for the 8-bit DAC, the resolution of the black level adjustment is equal to 2/256=8mV.

2) Long cut-off convergence time when the TV set is switched on.
In a worst case, 256 steps are required for the conventional cut-off loop circuit to reach a stable state. Since the conventional circuit works at the frame frequency, the time that must be allowed for the loop circuit to reach its convergence point is about 256*1/50=5 seconds (assuming a frame frequency equal to 50HZ).

3) No RGB output blanking is provided when the cut-off control loop is not stable.
When the cut-off control loop is not stable, the conventional circuit does not blank the RGB output. In this instance, the picture on the screen is not stable, and the colour may change. Pictures with strong colorimetry errors can therefore result.

Figure 4 is a block diagram of a digital cut-off control loop circuit for one channel of an RGB output controller, in accordance with a preferred embodiment of the present invention. Once again, in the drawing, only the BLUE channel circuitry is shown, and the red and green channel circuits will in practice be essentially the same. The circuit includes a number of

improvements over the conventional cut-off control loop circuit described above, and some of the improved features are discussed hereinbelow:

1) The simple comparator is replaced by a set of comparators (speeding comparator), indicating how far the loop is from a stable solution.

2) An additional speeding circuit is included which can generate the RGB output blanking signal while the cut-off control loop is not stable.

3) The 8-bit up-down counter is replaced by the 9-bit up-down counter.

4) The 8-bit DAC is replaced by the 9-bit DAC.

The working principle of the improved circuit is quite similar to the above described conventional circuit, however the relatively simple additional features provide very advantageous effects in overcoming or reducing the problems discussed above. The improved circuit uses a 9-bit up-down counter and a 9-bit DAC to replace the 8-bit up-down counter and the 8-bit DAC of the conventional circuit, in order to increase the resolution of the black level adjustment. Ordinarily this would result in an even longer convergence time for the loop circuit to determine a stable cut-off voltage. However, the improved circuit also employs a speeding comparator in place of the simple comparator of the prior art, and adds a speeding block to reduce the time required to reach stability when the TV set is switched on.

The speeding comparator comprises of six parallel comparators arranged with different comparison voltages spread over an operative range. The output of the speeding comparator is fed to a speeding logic circuit which is interposed between the comparator and the up-down counter. The combination of speeding comparator and logic circuit are used to reduce the convergence time of the cut-off control loop circuit. The speeding comparator produces an output which is dependant upon the level of the *ICAT* voltage within the operative range.

Based on the speeding comparator output, the speeding logic circuit produces an output to the up-down counter to vary the output thereof up or down. Depending upon how far away from the stable voltage the circuit is, as indicated by the speeding comparator output, the logic circuit instructs the counter to increase or decrease by a greater or lesser amount. The combined function of the speeding comparator and logic circuit is best illustrated in Table 1, presented below.

If the voltage on the *ICAT* pin is far away from 2V, that means the cut-off control loop is not stable, and the speeding comparator and the speeding logic circuit will therefore produce a signal to the 9-bit up-down counter to increase or decrease the output current of the cut-off control loop at 4-times the standard speed. This enables the improved cut-off control loop circuit to reach stability in a greatly reduced time, despite using a higher resolution counter and DAC. In order to avoid the need to increase the clock, the speeding is obtained by modifying the bits LSB+1 or LSB+2 of the Up/Down counter.

The speeding logic circuit also produces a RGB output blanking signal to blank the RGB output. RGB output blanking bypasses the counter and DAC portion of the loop circuit to blank the RGB output when the cut-off control loop is not stable. The stability of the cut-off control loop is judged by the speeding logic circuit on the basis of the speeding comparator output, as discussed above. Thus, the improved circuit will blank the RGB output whilst the cut-off control loop is unstable, so the picture on the screen is not seen, which is better for TV set. This is done again, using the outputs of the comparators, as an indication of how close or far from convergence the loop is. As this information is only available during the cut-off lines, it is needed to memorize the blanking status, until the next operation of the loop.

In the improved circuit the speeding logic circuit operates to blank the RGB output if any of the three RGB channels has its cut-off loop operating at the highest counting speed (+/- 4 bits). This is a compromise between providing blanking until all 3 channels have converged (but a long blanking time), and a short blanking time (but the display of pictures with still some colorimetry errors).

Since the 8-bit DAC of the conventional circuit is replaced by a 9-bit DAC, the resolution of the black level adjustment is increased. Generally, the range of the black level adjustment is about 2V, and since, in the improved circuit, there is a total of 512 steps for the 9-bit DAC, the resolution of the resulting black level adjustment is 2/512=4mV. In worst case, when the TV set is switched on it requires 512 steps for the cut-off control loop circuit to reach a stable state. Since the cut-off control loop works at the frame frequency, the worst case stability time is therefore about 512*1/50/4=2.5 seconds. Without the speeding circuit, the worst case stability time would be 10 seconds, which is considered too long for the user.

Table 1: The function of the speeding comparator and speeding circuit

Icat input voltage (V)	Output of the Speeding Circuit
> 2.126	down 4 bits
2.046 ~ 2.126	down 2 bits
2.006 ~ 2.046	down 1 bit
1.994 ~ 2.006	stable
1.954 ~ 1.994	up 1 bit
1.874 ~ 1.954	up 2 bits
<1.874	up 4 bits

The stable output represent a "dead zone" in order to avoid digital oscillation of the outputs, and is chosen so that at least 1 step falls inside this voltage range.

An exemplary implementation of the speeding logic and up/down counter circuitry is shown in schematic block diagram form in Figure 5, and the operation of the circuit is described hereinbelow and contrasted with the form of counter employed in the prior art applications. The circuit shown in Figure 5 includes nine counter cells which provide respective D outputs (D_0, D_1, ... , D_8) to the 9-bit DAC. In the prior art, eight cells are employed and coupled in a serial arrangement with two clocks (Ck1 for counting up and Ck2 for counting down) provided as input to the least-significant-bit cell. The cells in the improved circuit illustrated

in Figure 5 is arranged in a generally similar construction, although including nine cells as previously mentioned, and speeding logic circuitry in the form of a collection of logic gates coupled amongst the three least-significant-bit cells.

In the prior art, two clocks are provided, one for counting up and another for counting down. For counting up, the clock Ck1 is propagated as input through the counter cells on high levels (D=1), until the first low level (included). For example, for a cell A, with input $Ck1_A$ and a previous cell (A-1), with output $D_{(A-1)}$, and input $Ck1_{(A-1)}$, the following logic equation arises: $Ck1_A = Ck1_{(A-1)}$ AND $D_{(A-1)}$. An example of this counter function is expressed in the table below:

	b_0	b_1								b_n
Counter value:	1	1	.	.	1	0	X	X	X	X
Clock:	C	C	.	.	C	C	0	0	0	0
On Ck1 (in) counter becomes:	0	0	.	.	0	1	X	X	X	X

All the bits where Ck1 propagation was allowed (bits with C flag), are flipped on, creating here a +1 case. Bits with status X are unchanged.

For counting down in the prior art construction, the clock Ck2 is propagated as input through the counter cells on low levels (D=0), until the first high level (included). For example, for a cell A, with input $Ck2_A$ and a previous cell (A-1), with output $D_{(A-1)}$, and input $Ck2_{(A-1)}$, the following logic equation arises: $Ck2_A = Ck2_{(A-1)}$ AND $D_{(A-1)}$. An example of this counter function is expressed in the table below:

	b_0	b_1								b_n
Counter value:	0	0	.	.	0	1	X	X	X	X
Clock:	C	C	.	.	C	C	0	0	0	0
On Ck2 (in) counter becomes:	1	1	.	.	1	0	X	X	X	X

All the bits where Ck2 propagation was allowed (bits with C flag), are flipped, creating here

a -1 case. Bits with status X are unchanged.

For the improved speeding counter circuit of Figure 5, three up/down counting speeds are provided. To achieve this, the clock is applied at the CkX (X = 1 or 2) clock input, of cell 0 (count +/- 1 for speed 1), cell 1 (count +/- 2 for speed 2), or cell 2 (count +/- 4 for speed 4), depending of the result of the speeding comparators. A set of memory cells, 1 per comparator (not represented in the diagram) will stabilize the status before the clock pulse, in order to avoid a double clock generated by change of status during the clock pulse.

Referring to Table 1 above, the following signals can be derived from the speeding comparator outputs:

Up_1 = "up 1 bit"

Up_2 = "up 2 bits"

Up_4 = "up 4 bits"

Dn_1 = "down 1 bit"

Dn_2 = "down 2 bits"

Dn_4 = "down 4 bits"

In order to achieve the multiple speed counting, the following logic equations can be utilised:

$Ck1_0 = Clock\ AND\ Up_0$

$Ck1_1 = (Clock\ AND\ Up_2)\ OR\ (D_1\ AND\ Ck1_0)$

$Ck1_2 = (Clock\ AND\ Up_4)\ OR\ (D_2\ AND\ Ck1_1)$

$Ck2_0 = Clock\ AND\ Dn_0$

$Ck2_1 = (Clock\ AND\ Dn_2)\ OR\ (NOT\ (D_1)\ AND\ Ck2_0)$

$Ck2_2 = (Clock\ AND\ Dn_4)\ OR\ (NOT\ (D_1)\ AND\ Ck2_1)$

These logic expressions are implemented in the speeding logic circuitry coupled to the counter cells illustrated in Figure 5

An example of the counter function of the speeding counter as shown, for the case of counting

up by increments of 4, is expressed in the table below:

	b_0	b_1	b_2							b_n
Counter value:	X	X	1	.	1	0	X	X	X	X
Clock:	0	0	C	.	C	C	0	0	0	0
On Ck1 (in) counter becomes:	X	X	0	.	0	1	X	X	X	X

Where "X" states are unchanged, and the clock propagation is indicated as "C".

Another example of the counter function of the speeding counter as shown, for the case of counting down by increments of 2, is expressed in the table below:

	b_0	b_1								b_n
Counter value:	X	0	.	.	0	1	X	X	X	X
Clock:	0	C	.	.	C	C	0	0	0	0
On Ck2 (in) counter becomes:	X	1	.	.	1	0	X	X	X	X

The improved cut-off control loop circuit described hereinabove can be advantageously implemented in an integrated circuit for inclusion in TV/video RGB control circuitry, and the actual design of the circuit components will be readily ascertainable by those skilled in the art from the foregoing functional description and accompanying drawings. It will be appreciated that the improved circuit can be extended to higher bit count, or increased number of comparators for even higher counting speeds or different values of the comparators. The limitation of higher bit count then is the complexity of the DAC, which needs to be monotonous for this application.

The foregoing detailed description of the present invention has been presented by way of example only, and is not intended to be considered limiting to the invention as defined in the accompanying claims. For example, the numerical quantitites presented herein such as the

2.0 volt cut-off reference voltage and the 1.75 volt leakage reference voltage, whilst valid for the embodiment described and illustrated, do not limit the present invention to those values, and the principles and structures of the invention can equally be adapted to applications with different voltages and using different valued components.

Claims:

1. An RGB control circuit for use in television/video display control, comprising:

a display driver current sensor;

a counter circuit and analog output circuit coupled to control the display driver current;

a speeding comparator having a plurality of comparator circuits coupled in parallel with the display driver current sensor as input, for determining and outputting a measure of the difference between the sensed display driver current and a predetermined value thereof; and

a speeding logic circuit coupled to the speeding comparator and counter circuit, and arranged to control the up/down counting rate of the counter circuit according to said measure of difference in display driver current.

2. An RGB control circuit as claimed in claim 1, wherein the speeding logic circuit is arranged to control the counting rate of the counter circuit, and thus the display driver current, based on the output of the speeding comparator so as to converge the display driver current to said predetermined value.

3. An RGB control circuit as claimed in claim 2, wherein said speeding logic circuit produces a RGB output blanking signal whilst said display driver current is substantially different from said predetermined value.

4. An RGB control circuit as claimed in claim 3, including control circuits for each of the colour channels, and wherein said speeding logic circuit produces said RGB output blanking signal based on the counting rate of any and/or each of the counter circuits for the colour channels.

5. An RGB control circuit as claimed in claim 1 or 2, wherein the speeding comparator has a plurality of outputs including a convergent output and at least one upper output and

lower output, and wherein said convergent output corresponds to said display driver current being substantially equal to said predetermined value and said upper and lower outputs are utilised by said speeding logic circuit to determine the up/down counting rate of the counter circuit.

6. An RGB control circuit as claimed in claim 5, wherein each of said upper and lower outputs correspond to respective up and down binary counting rates for said counter circuit.

7. An RGB control circuit as claimed in claim 1 or 2, wherein the up/down counter and analog output circuit are both 9-bit circuits.

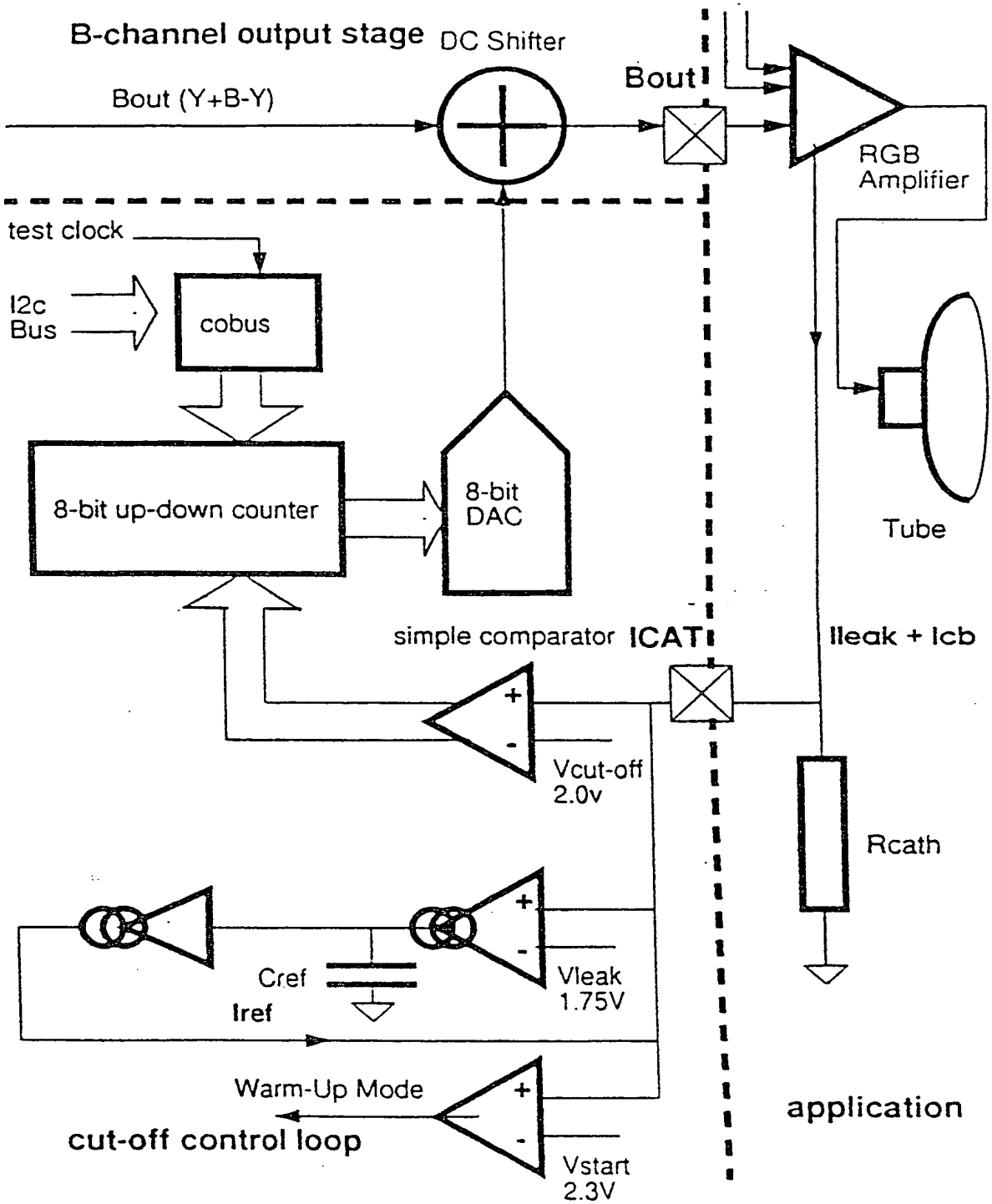

B-channel output stage
DC Shifter
Bout (Y+B-Y)
Bout
RGB Amplifier
test clock
I2c Bus
cobus
8-bit up-down counter
8-bit DAC
Tube
simple comparator
ICAT
Ileak + Icb
Vcut-off 2.0v
Rcath
Cref
Iref
Vleak 1.75V
Warm-Up Mode
cut-off control loop
Vstart 2.3V
application

Fig 1

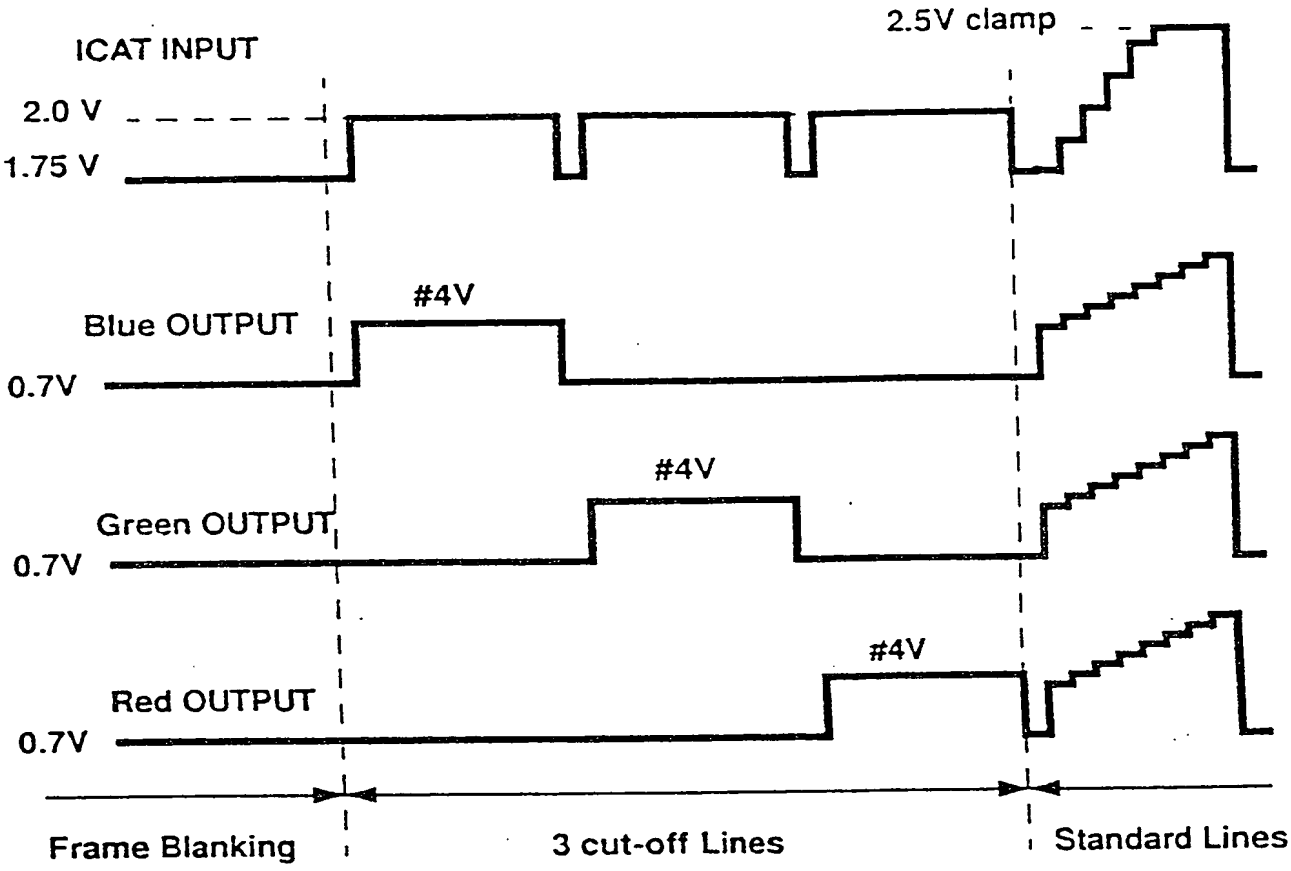


Fig 2: Waveforms at the RGB outputs and Icath input during the cut-off measurements lines

Waveforms at the RGB outputs during warm-up detection mode

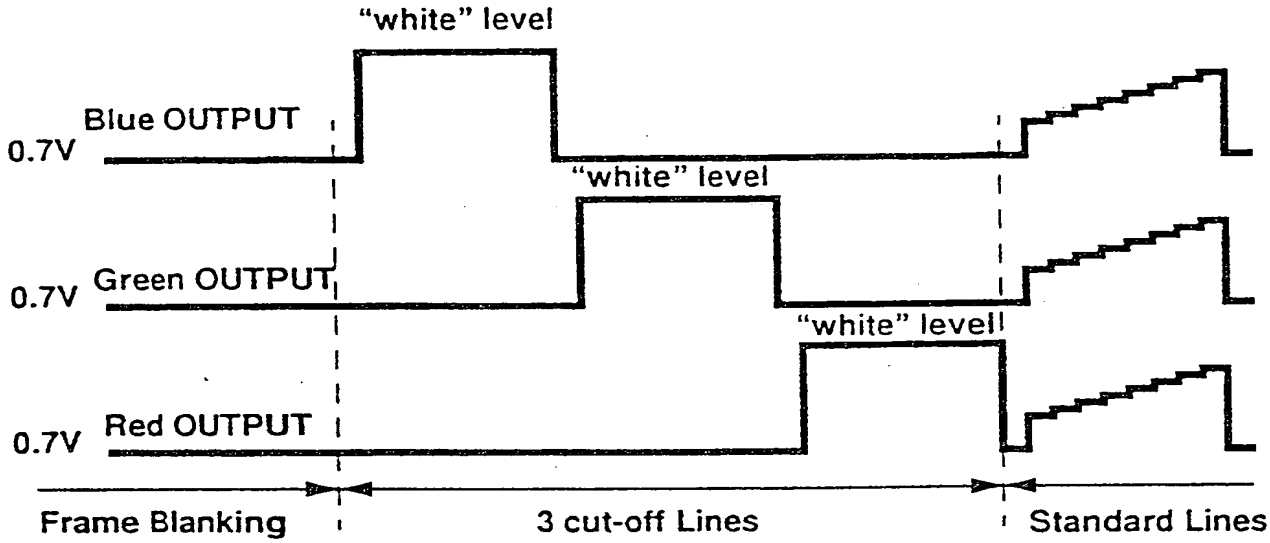


Fig 3: Waveforms at the RGB outputs during warm-up detection mode

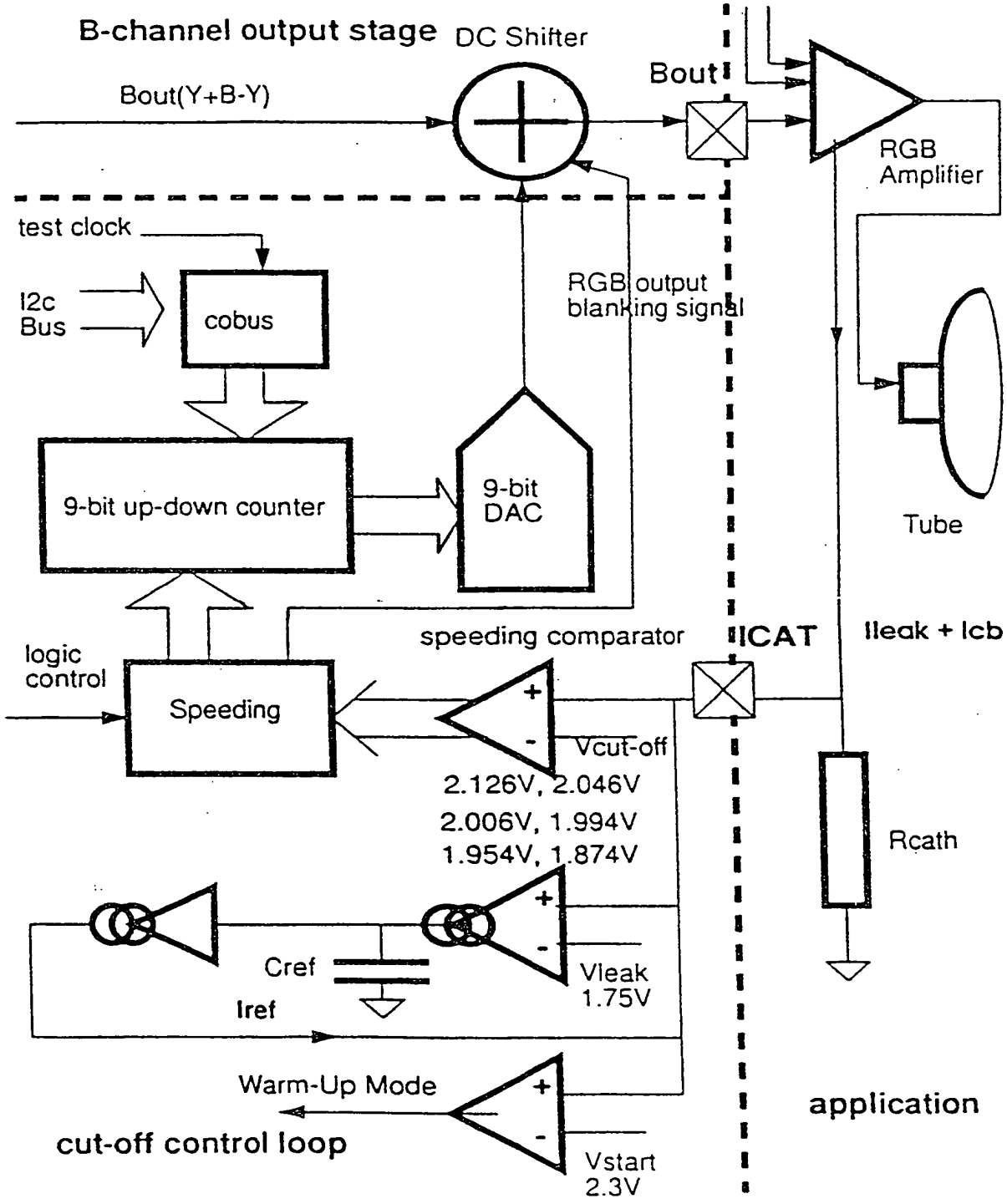

B-channel output stage
DC Shifter
Bout
Bout(Y+B-Y)
RGB Amplifier
test clock
I2c Bus
cobus
RGB output blanking signal
9-bit up-down counter
9-bit DAC
Tube
speeding comparator
ICAT
Ileak + Icb
logic control
Speeding
Vcut-off
2.126V, 2.046V
2.006V, 1.994V
1.954V, 1.874V
Rcath
Cref
Iref
Vleak 1.75V
Warm-Up Mode
application
cut-off control loop
Vstart 2.3V

Fig 4

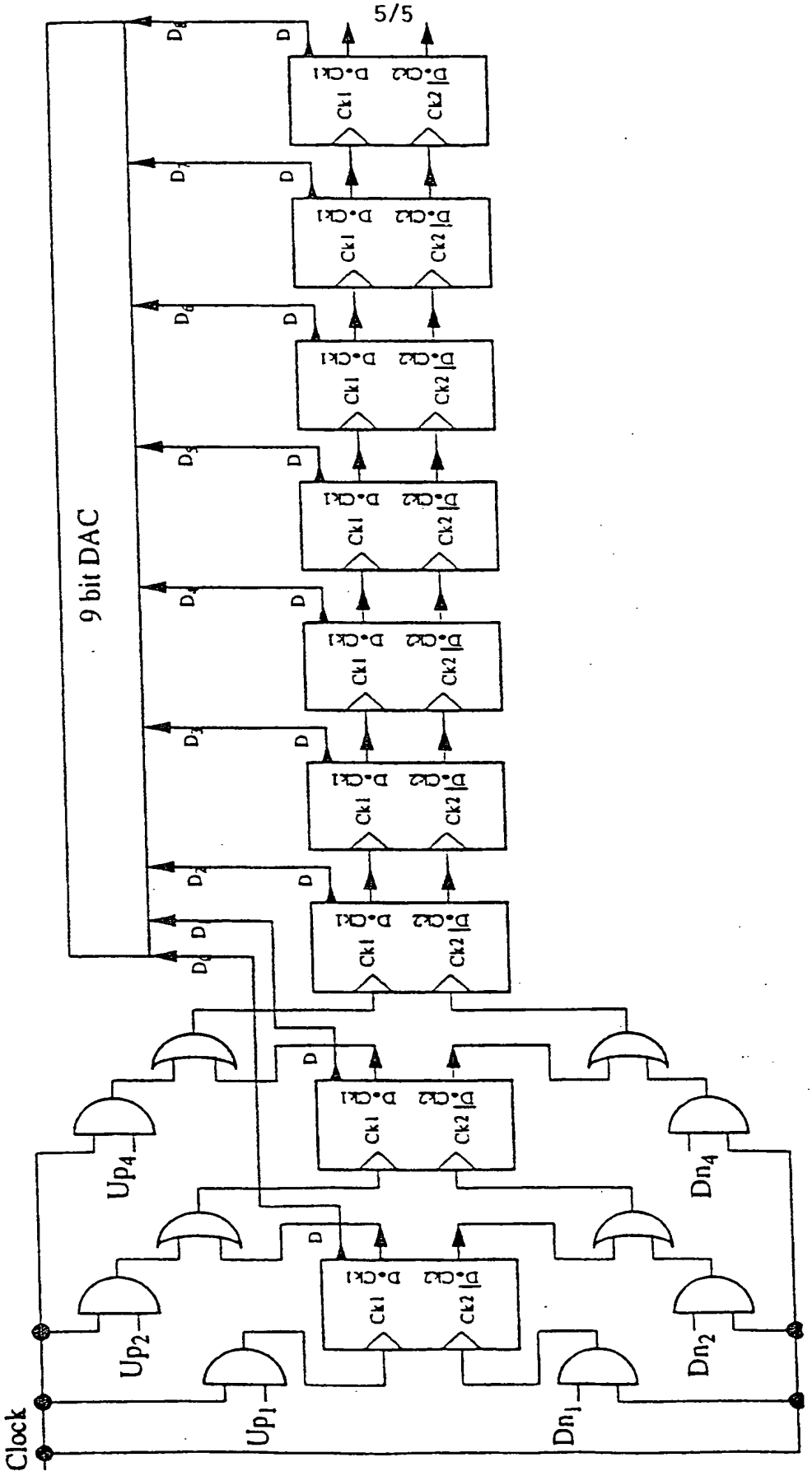


Fig 5

INTERNATIONAL SEARCH REPORT

International Application No
PCT/SG 98/00076

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04N9/64 H04N9/72

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 339 011 A (TAMURA TAKAHIKO ET AL) 16 August 1994 see column 11, line 29 - column 12, line 42; figures 1,13,14 ---	1-4
X	GAY M J: "DIGITALLY CONTROLLED VIDEO PROCESSOR WITH ACCURATE GREY-SCALE" IEEE TRANSACTIONS ON CONSUMER ELECTRONICS, vol. 38, no. 2, 1 May 1992, pages 91-100, XP000301633 see page 93, left-hand column see page 99, right-hand column, line 18 - line 30 --- -/--	1-4

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 February 1999	19/02/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Bequet, T

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/SG 98/00076

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropnate, of the relevant passages	Relevant to claim No.
A	DOUZIECH P ET AL: "A LARGE-BANDWIDTH VEDEOPROCESSOR FOR HIGH DEFINITION AND DOUBLE-SCAN TV SETS" IEEE TRANSACTIONS ON CONSUMER ELECTRONICS, vol. 37, no. 4, 1 November 1991, pages 928-931, XP000276019 see page 930, left-hand column, line 1 - right-hand column, line 25 ---	1
A	US 4 689 665 A (JOHANNES KURT J ET AL) 25 August 1987 see column 1, line 46 - column 2, line 10 -----	1

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/SG 98/00076

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5339011 A	16-08-1994	JP 5236500 A	10-09-1993
US 4689665 A	25-08-1987	DE 3438564 A	30-04-1986
		EP 0179526 A	30-04-1986
		JP 1908973 C	24-02-1995
		JP 6038667 B	18-05-1994
		JP 61100088 A	19-05-1986